Sea Level Failures of Power MOSFETs Displaying Characteristics of Cosmic Radiation Effects

R. Sheehy, J. Dekter, N. Machin
Rectifier Technologies Pacific Pty. Ltd.
24 Harker st, Burwood 3125, VIC, Australia

***Abstract* - An investigation into the failure rate of Power MOSFETs with room temperature junctions has been performed at sea level covering a range of drain voltages up to 110% of device rating. Phenomenally high failures rates over 10% per week were recorded using a test arrangement where the devices were configured to block continuous forward DC voltage. The failure rates were found to be several orders of magnitude higher than the expected Arrhenius model rate and were found to have a maximum near room temperature. The data was found to exceed the estimated sea level Single Event Burnout and Single Event Gate Rupture described in recent space and avionics radiation research papers, at greater than 80% voltage stress. Experimental data and the test arrangements are described, along with an empirical equation for reliability prediction.**

I. INTRODUCTION

A common belief held among the power electronic community is that the reliability of power MOSFETs increases as the junction temperature reduces. Consequently, reliability figures for electronic products are frequently calculated at room temperature. Power devices are often operated at low junction temperatures to increase the predicted lifetime of products, especially in ultra-conservative design. This ideology assumes that there are no failure mechanisms that become worse as junctions approach room temperature. Evidence of this is the high temperature (125°C) reverse bias tests commonly performed by semiconductor manufacturers to characterize the expected reliability of power devices, with the explicit assumption that lifetimes increase with reduced junction temperatures.

Two Arrhenius based models used to predict reliability of power MOSFETs assume that failure mechanisms that lead to random failure become worse with increasing temperature and applied power stress [1,2]. There is no random failure mechanism specified for MOSFETs as a function of applied voltage stress in these models.

Some additional failure mechanisms not covered by the Arrhenius based reliability models can be removed by design, by reducing the applied switching and/or peak voltage stress. These failure mechanisms for power MOSFETs have been documented [3-15], most of which concern the inadvertent turn-on of the parasitic bipolar transistor inherent in all MOSFETs. Mechanisms such as dv/dt induced secondary breakdown of the parasitic bipolar transistor after body drain diode conduction [3-5], and di/dt activation of the parasitic bipolar transistor during body diode reverse recovery [5,6] have been well documented.
Other mechanisms like Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR) were first reported in space applications research [7-13] and Avionics field failure analysis [14,15] and are now well documented. The SEB and SEGR mechanisms are not well known in the terrestrial power electronics community, possibly because of the perception that the surface of the earth is relatively benign with respect to high-energy cosmic particle flux. Several recent papers have shown that the radiation effects seen in space and at high altitude are also seen at sea level with a reduced incident rate [10-12]. Additionally, a number of terrestrial failures of MOSFETs, IGBTs, GTOs, and high voltage diodes have been attributed to SEB and SEGR, suggesting the most likely cause to be high-energy cosmic particles or their associated secondary radiation of atmospheric neutrons [12-14].

SEB in a MOSFET occurs when a high energy particle passes through the parasitic bipolar transistor region of the semiconductor die. A plasma filament of hole-electron pairs along the path of the particle is generated. The parasitic bipolar transistor is turned on in a tiny region, and if applied voltage stress is high enough, will regeneratively increase the local current until burnout occurs.

SEGR occurs when a high energy particle passes through the gate oxide region of the MOSFET, generating a plasma filament of hole-electron pairs between the gate oxide and drain. This intensifies the electric field between gate oxide and channel region. If the applied drain voltage is high enough, the gate oxide will rupture locally, especially if the gate voltage is zero or negative.

For detailed explanations of these mechanisms, see papers by Johnson, et al. [13] and Normand, et al. [12] for SEB and Wheatley, et al. [9] for SEGR.

It is the authors' view that the failures reported in this paper are accounted for by the SEB and SEGR mechanisms. The objective of this paper is to present this data and knowledge to the wider power electronics community, and to present an empirical failure prediction model to facilitate designs that are more reliable.

In the recent publication by Galyon et al. [16], power MOSFETs operating at room temperature blocking constant DC for long periods were reported to randomly fail catastrophically. The analysis of the failure sites on the chip area concluded that the failure locations were random and that the failures occurred within the array of mini-FETs distributed throughout the chip area. This was termed an 'array failure' and was characterized by a relatively small black area on the die where the metallization had alloyed with the underlying silicon. The paper also reported that

laboratory testing of devices under the same operating conditions showed failure rates of approximately 6% per week and observed that the failure symptoms were consistent with SEB.

At Rectifier Technologies Pacific (RTP), a program of Static Reverse Bias (SRB) testing was undertaken, testing different high voltage power MOSFET devices with ratings ranging from 500V to 1200V from several manufacturers. A failure rate of five orders of magnitude higher than the expected Arrhenius rate was observed. For one 1000V device tested, a temperature dependence that peaks around 30°C and falls with increasing temperature was observed. The paper describes the test circuits used, the types of devices investigated, the results and their implications. The final section presents an empirical failure prediction equation and a design example for a phase shifted full bridge converter.

II. EXPERIMENTAL PROCEDURE - NON-DESTRUCTIVE STATIC REVERSE BIAS TESTING

A regulated DC voltage is applied to the test cell of Fig. 1, which results in a static electric field across the MOSFET drift region. The gate-source voltage is held at zero volts via the 10 ohm resistor. The complete rig consists of many test cells in parallel. Anything that would produce an unpredicted current spike through any test cell is classed as an "event". When an event occurs in a MOSFET, the drain-source voltage in the affected cell can completely collapse while limiting external drain current in an effort to prevent catastrophic device failure. The drain-source voltage of other cells are unaffected by the event. Fig. 2 shows a typical current waveform in a test cell recorded as a voltage across Rs as a result of such an event.

The waveform has the following two salient features:

- The voltage across Rs rises rapidly in several hundred nanoseconds, to the limiting value corresponding to a shorted device.
- A slight increase in the current after the initial rapid rise is followed by a slow decay towards zero.

To explain the observed waveform, a Pspice simulation was done with the equivalent circuit shown in Fig. 3. The external parallel resistor and capacitor simulates the effect of 140 test cells in parallel. Fig. 4 shows the simulation result, revealing a high degree of similarity to the observed waveform. The simulation confirms that the observed waveform can be explained by a single device rapidly turning on, and turning off as soon as the drain to source voltage has collapsed to close to zero volts, within less than 1µs. The slight increase in current before the decay, as well as the decay itself, are due to the combined effect of the other test cells in the circuit.

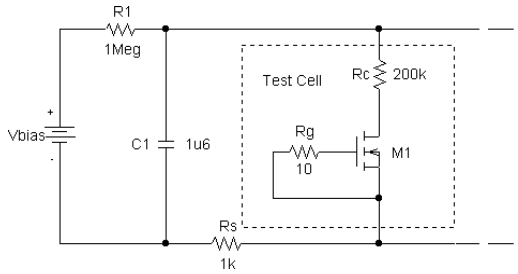

Fig. 1 Basic test cell used to detect events.

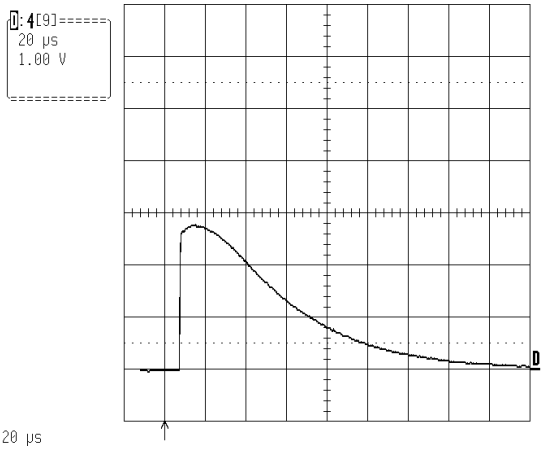

Fig. 2. Event current waveform.

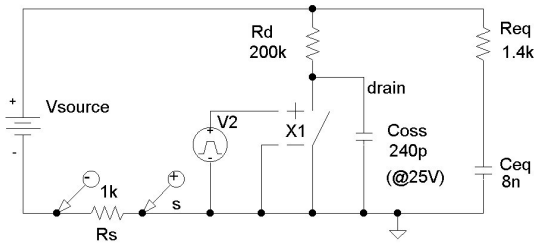

Fig. 3. Equivalent circuit model of the test rig during an event

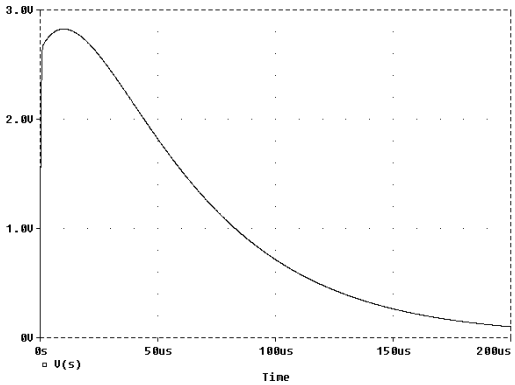

Fig. 4. Pspice simulation of equivalent circuit event current detected by the current sense resistor

III. EXPERIMENTAL RESULTS

Using a test rig containing up to 500 test cells in parallel, a number of power MOSFETs rated from 500V to 1200V were tested at various voltage stresses of up to 110% of the manufacturers' specified device rating. Current spikes through Rs were counted as events. Devices with different die sizes from different manufacturers (labeled A, B and C in Fig. 5) were used with test populations varying from 50 to 500 devices per test. Because of the length of time required to get events at lower voltage stresses, only a few of the devices were tested below 90% of the device rating. Tests were conducted at between 20 and 25°C.

Fig. 5 shows the results of more than 1 million device-hours of testing. The results are normalized with respect to die size and applied voltage. This allows comparison between different device types and technologies under the assumption that event rate is directly proportional to die size. Also, plotting the data points as a function of applied stress as a percentage of rated voltage, allows comparison between devices with different voltage rating. The strong correlation obtained demonstrates the validity of this approach.

Each data point is shown with error bars indicating the 90% confidence limits, according to the Poisson distribution. The plot also shows the baseline Arrhenius failure rate used for MTBF calculations for a 25°C junction, which is independent of die size or device voltage rating. Event rate is taken to be directly equivalent to failure rate.

There are several striking points in this figure:

- There is a large degree of similarity in failure rate between devices, independent of manufacturer or voltage rating. There is a general band in which almost all measured rates fall.
- There is a group of devices from manufacturer A that fall outside this general curve. These devices all have 500V rating. This is discussed in more detail in section IV.
- At 100% voltage stress, the failure rate of devices that fall in the general band was more than 10,000 times higher than the Arrhenius model random failure rate.

These results are highly repeatable. Some devices have been re-tested at different times, with error bars of different tests overlapping in all cases.

Fig. 6 shows failure rate (not normalized) as a function of junction temperature for a 1000V device at 97% voltage stress. A peak failure rate is observed at 30°C that decreases approximately by a factor of 10 at 80°C.

During these tests, it was observed that despite the non-destructive nature of the test cell, in some cases devices still fail catastrophically. This is manifested either by an increase in the device leakage current by several orders of magnitude, or by a low resistance between gate and source on the order of 20 to 100 ohms. These two cases correspond to SEB and SEGR [9] effects respectively.

Some devices were more susceptible to catastrophic failure in the tests. In particular, 1000V devices from manufacturer A suffered catastrophic failure more often compared with their 500V devices at similar stress levels. Roughly 10% of events resulted in catastrophic failure at 97% stress. Most of those failures exhibited symptoms consistent with SEGR, that is a low resistance between gate and source. Catastrophic failure in 1000V devices was not observed at a reduced bias voltage, despite events still occurring.

Another observation concerning a population of 600V superjunction MOSFETs from another manufacturer at 95% stress, was that every single event recorded resulted in a catastrophic failure of the device. All those cases exhibited symptoms consistent with SEB.

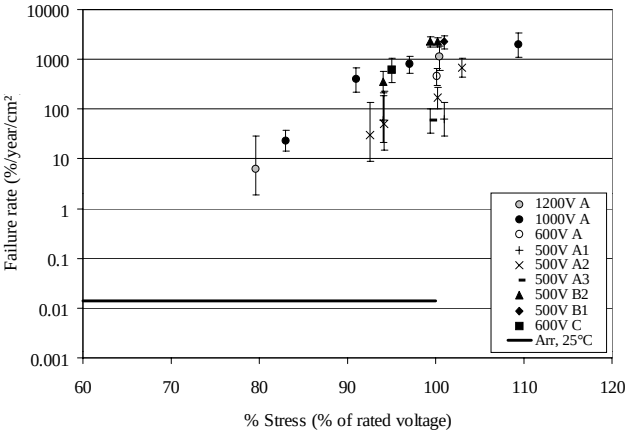

Fig. 5. Normalized device failure rate.

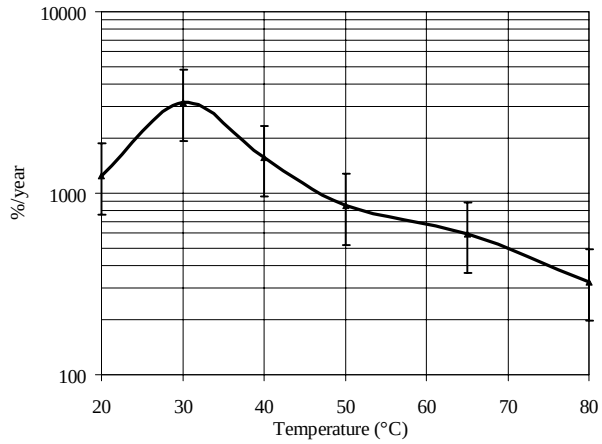

Fig. 6 Failure rate as a function of junction temperature.

IV. Discussion of results

Examination of devices that have undergone catastrophic failure in the test rig show local point defects. Such failures are consistent with SEB and SEGR.

Fig. 7 and Fig. 8 show two examples of such failures. Both cases indicate melting of the aluminium and subsequent squeezing out of the structure via the contact hole. Failure sites occur randomly in the active area.

It is assumed that every event recorded in the non-destructive tests would have resulted in catastrophic failure if the available energy was high enough. This assumption was validated in the early stages of testing, when a different test cell with much higher available energy was used. During those tests, every event resulted in a catastrophic failure. When the energy was reduced by using the described test rig, events continued at the same rate. (These early results are not included in the data in this paper.)

During an SEB event, the region in a MOSFET that briefly turns on is the parasitic bipolar transistor [13]. This would explain the observation that the drain to source voltage must collapse to a small percentage of the bias value before the device can recover.

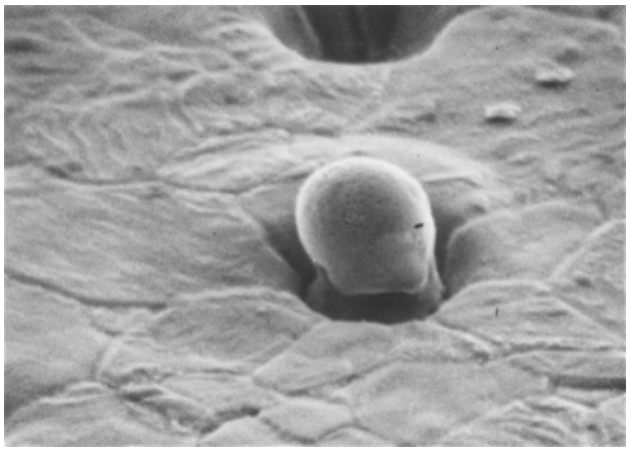

Fig. 7 Superjunction MOSFET failure site.

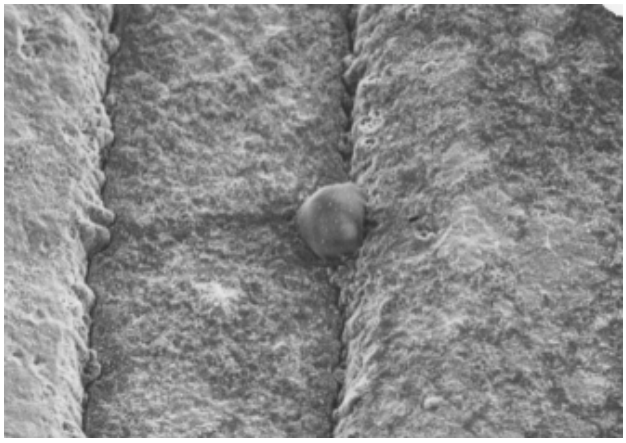

Fig. 8 Strip MOSFET failure site.

The group of points of 500V devices (A1, A2 and A3) in Fig. 5 that are below the main band can also be explained by the above hypothesis. These devices have reduced parasitic bipolar transistor gain apparently resulting in improved immunity to SEB. Other manufacturers' 500V devices apparently do not have this characteristic as evidenced by the results for those devices falling in the main band.

The assumption that event rate is proportional to die size is based on the premise that the mechanism is SEB and SEGR. This implies that each die acts as a particle detector, hence the bigger the die, the higher the probability that a die will detect a particle. Therefore, if SEB and SEGR are the dominant mechanisms, normalising the data with respect to die size should result in a strong correlation independent of die size. The strong correlation in the data supports this hypothesis.

Previous studies of sea level failures of high voltage devices (>1000V) were found to fall to zero when the tests were performed 500 feet underground in a salt mine [17], indicating the influence of high energy cosmic particles. High-energy neutron, proton and ion flux data have been compiled by Boeing and NASA and some areas above the earth have significantly higher levels of particle flux, such as the South Atlantic Anomaly [18].

V. Predicting Failures

Fig. 9 shows the RTP data points and line of best fit along with a prediction by Oberg et al. [9] for power MOSFETs for SEB at sea level. The error bars have been omitted for clarity. The measured rate published by Galyon et al. [15] has also been included. No device die size was published in that case, but 0.7 cm² was estimated for normalization. Die sizes range from about 0.5cm² to 1.5cm² for typical devices.

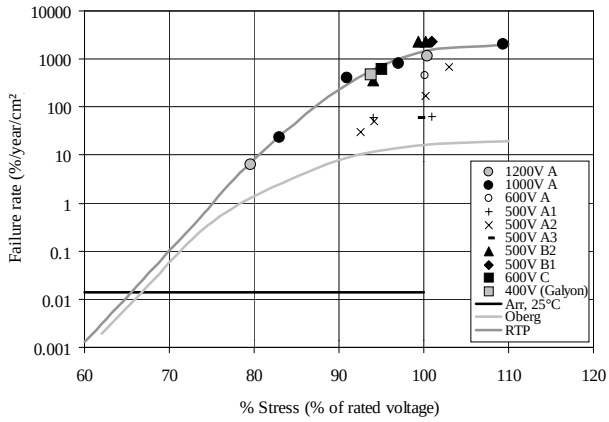

Fig. 9 Data with prediction by Oberg et al., and prediction by RTP.

Although the shape of the general failure curve agrees with the prediction by Oberg, the measured failure rate is significantly higher than the Oberg prediction at high stress levels. Oberg's prediction is based on accelerated tests using a neutron source for bombardment and not field data,

and the two sets of data from Oberg and RTP do not overlap in the applied stress range. This may be the explanation for the discrepancy.

The best fit curve is purely an empirical curve based on test data. For practical purposes, a simple power law approximation of the failure rate per year is given by

$$failure\_rate = 10^{(0.19 \times Vstress\,\% - 14.3)}\ [\%\bullet year^{-1}\bullet cm^{-2}] \quad (1)$$

where *Vstress*% is the percentage of rated voltage stress applied. The saturation effect at stress higher than 85% is not reflected in the equation. For example, the equation predicts 1% failure rate per year per cm² at 75% stress. As a first approximation, if the voltage stress in the device off-state is less than 85%, the failure rate decreases by a factor of 100 for every 10% decrease in the voltage stress. This huge rate of decrease indicates that every volt reduction has to be considered in marginal cases, and as a general rule, 75% stress should not be exceeded.

Since the energy in real applications such as switchmode power supplies is almost always higher than in the test rig, it can be assumed that the rate measured can be extrapolated to predict the actual failure rate. The switch duty cycle and the instantaneous voltage over a switching cycle needs to be taken into account to arrive at a valid failure rate.

It is important to note that even though MOSFETs are rated for avalanche operation, the probability for catastrophic failure when operated near or in avalanche mode is high, regardless of the circuit energy available. High voltage MOSFETs especially should never be used in avalanche mode.

There is evidence that the rate falls off with increasing temperature. Fig. 6 shows a factor of 10 reduction between 30°C to 80°C, while some evidence [12] suggests that this effect is dominant at lower stress levels, reducing the failure rate to negligible levels when the junction is hot.

The failure rate should increase at higher altitudes due to the increased flux of high energy particles. Similarly, a variation in particle flux occurs with latitude, reducing by a factor of 4:1 from poles to the equator [15, 17, 18]. The RTP tests were done near 38° south.

To demonstrate a practical application of equation (1), consider a phase-shifted full bridge converter operating from a DC input voltage of 400V. The typical duty cycle for such a design would be 0.5 for each switch. If IRFP460 (500V) devices were used, the predicted failure rate for each switch is

$$failure\_rate = 0.5 \times 10^{(0.19 \times 80 - 14.3)}$$

= 3.97% per year per cm² of silicon.

Since there are 4 devices in the bridge of 0.62cm² each, the total rate would be 10% per year. This example highlights an unexpected problem with the phase-shifted full bridge topology, that the duty cycle remains at 0.5 for all loads. Other topologies would reduce the switch duty cycle at light load, alleviating the problem to some extent.

If 600V devices were used instead, the total rate would decrease to 0.05% per year, well below typically expected product failure rates.

This is applicable only for cases where the junctions are cool. In addition, there are other factors that may play a role in reducing the failure rate, such as physical orientation and shielding by the surrounding building, especially if there is a significant amount of soil or concrete overhead [12].

VI. Conclusion

It has been shown that MOSFET circuits that are operating at room temperature and greater than 65% applied voltage stress, can experience unexpectedly high failure rates at sea level. The actual failure rate can be several orders of magnitude higher than the failure rate predicted by the Arrhenius models. Previous aerospace and avionics research indicates that the most likely cause for these failures is due to SEB and SEGR caused by atmospheric neutrons and other cosmic particles. Based on experimental data, a new empirical prediction model is proposed which should be applied to designs using MOSFETs at sea level which are running cool junctions and peak voltage stress levels above 65%.

Acknowledgments

The authors wish to thank J. Hess and G. Wright of Advanced Power Technologies for their assistance in obtaining SEM images, many discussions on device physics and assistance in obtaining reference material.

References

[1] Telcordia Technical Reference TR-332/1997, *Reliability Prediction Procedure for Electronic Equipment*, Telcordia Laboratories

[2] MIL-HDBK-217F, *Military Handbook - Reliability Prediction Of Electronic Equipment,* Dec 1991, US Department of Defense

[3] D. L. Blackburn, "Turn-off failure of Power MOSFETs", IEEE Trans. Power Electronics, Vol. 2, No. 2, May 1988, pp. 136-142.

[4] L. Saro, K. Dierberger, R. Redl, "High-Voltage MOSFET Behaviour in Soft-Switching Converters: Analysis and Reliability Improvements", *Proc. 24th IEEE Intelec 1998*, San Francisco, USA, Paper 2-2, pp. 30-40.

[5] G. Busatto, G. V Persiano, F. Iannuzzo, "Experimental and Numerical Investigation on MOSFET's Failure During

Reverse Recovery of its Internal Diode", IEEE Trans. Electron Devices, Vol. 46, No. 6, June 1999, pp.1268-1273.

[6] N. Keskar, M. Trivedi, K. Shenai, "On the Reliability of DC-DC Converters", Proc. Intelec 1999, pp. 1639-1645.

[7] A. E. Waskiewicz, J. Groninger, V. H. Strahan, D. M. Long, "Burnout of Power MOS Transistors with Heavy Ions of Californium-252", IEEE Trans. Nucl. Sci., Vol 33, 1986, pp. 1710-1716.

[8] J. L. Titus, C. F. Wheatley, "Experimental Studies of Single Event Gate Rupture and Burnout in Vertical Power MOSFETs", IEEE Trans. Nucl. Sci., Vol. 43, No. 2, April 1996, pp 533-545.

[9] C. F. Wheatley, J. L. Titus, D. I. Burton, "Single-Event Gate Rupture in Vertical Power MOSFETs; An Original Empirical Expression", IEEE Trans. Nucl. Sci., Vol. 41, No. 6, December 1994, pp. 2152-2159.

[10] D. L. Oberg, J. L. Wert, E. Normand, P. P. Majewski, S. A. Wender, "First Observations of Power MOSFET Burnout with High Energy Neutrons", IEEE Trans. Nuclear Science, Vol. 43, 1996, pp. 2913-2920.

[11] H. R. Zeller, "Cosmic Ray Induced Breakdown in High Voltage Semiconductor Devices, Microscopic Model and Phenomenological Lifetime Prediction", Proc. 6th International Symposium Power Semiconductor Devices & ICs, Germany, 1994.

[12] E. Normand, J. L. Wert, D. L. Oberg, P. P. Majewski, P. Voss, S. A. Wender, "Neutron-induced Single Event Burnout in High Voltage Electronics", IEEE Trans. Nuclear Science, Vol. 44, Dec 1997, pp. 2358-2366.

[13] G. H. Johnson, R. D. Schrimpf, K. F. Galloway, R. Koga, "Temperature Dependence of Single-Event Burnout in N-Channel Power MOSFETs", IEEE Trans. Nuclear Science, Vol. 39, No. 6, December 1992, pp. 1605-1612.

[14] A. Taber, E. Normand, "Single Event Upsets in Avionics", IEEE Trans. Nuclear Science, Vol. 40, No. 2, Apr. 1993, pp. 120-126.

[15] E. Normand, T. J. Baker, "Altitude and Latitude Variations in Avionics SEU and Atmospheric Neutron Flux", IEEE Trans. Nuclear Science, Vol. 40, No. 6, Dec 1993, pp. 1484-1490.

[16] G. T. Galyon, J. Cardinal, P. J.Singh, J. Newcomer, W Lorenz, K Chu, "Static and Dynamic Testing of Power MOSFETs", 16th Annual IEEE APEC, 2001, Vol. 1, pp 230-237.

[17] H. Kabza, et al., "Cosmic Radiation as a Cause for Power Device Failure and Possible Countermeasures", presented at 6th International Symposium on Power Semiconductor Devices and ICs, Davos Switzerland, May 1994, pp 9-12.

[18] M. Casolino, V. Bidoli, et.al, "Cosmic ray measurements on board space station MIR with SILEYE-2 experiment", Proc. 27th International Cosmic Ray Conference, Hamberg, Germany, 2001, pp.4011-4014.